IN THE SPECIFICATION:

Page 4, sixth paragraph that continues to page 5, REPLACE as follows:

These and other objects, features, and advantages are achieved in a programmable driver/equalizer with an alterable FIR circuit for equalizing serial links or other transmission systems to adapt to a variety of transmission media and impairments, specifically, InterSymbol Interference (ISI). Current mode differential drive circuits are coupled to a transmission media via a Finite Impulse Response (FIR) filter operating in a Z transform mode. The filter transfer function is of the general form of $H(Z) = Ab_0 + Ab_1Z^{-1} + AB_2Z^{-2} + \ldots AB_nZ^{-n}$ where the values of the coefficients [b_{-n}] **B_{-n}** are negative. The numerical value of the coefficients are set by register values in A and B coefficient setting circuits connected to the transmission line at the output of the drivers. The driver circuits include A coefficient level compensation and B coefficient level compensations for self-induced ISI from the driver while the filter coefficients are activated. The driver includes logic to reduce ISI by switching "off" high capacitance nodes when the filter coefficients are inactive. A bias circuit for the driver is coupled to a current mirror, which feeds a reference current from the bias circuit to the filter and logic circuit. The alterable filter circuit comprises A and B ~~delay circuits,~~ delay circuits for each coefficient being additively connected together between the input and the output of the past inputs and outputs while providing an output signal which is inverse of the transmission system. Each delay in the filter is realized by a shift register which stores the current outgoing data bit and a history of three previous bits. The output equals a preceding input as represented by the stored bits in the shift register. By setting the coefficients of the filter independently over a range which is controlled by a series of matched current sources; good tracking of the coefficients of the FIR is achieved, which enables the driver to adapt to a variety of transmission media and impairments.

Page 7, second paragraph that continues to page 8, REPLACE as follows:

The driver 100 provides OUT and OUTN (true and complement) to the transmission line 114. The Finite Impulse Response filter 116, to be described in Figure 4, includes an A coefficient driver setting circuit 118 and a B coefficient driver setting circuit 120. Each coefficient setting circuit is biased by the mirror end supply 104. Programmable A1, A2, and ~~A3~~ **A4** input control signals 122 are provided to the A coefficient circuit 118 and programmable B1,

B2, and ~~B3~~ **B4** input control signals 124 are provided to the B coefficient setting circuit 126. The A coefficient driver setting circuit is responsive to the Q1 true and QIN control signals 126 and 128 for clocking of the differential current amplifiers in the driver and power setting circuit 102. Likewise, the B coefficient setting circuit is responsive to Q4 true and Q4N control signals 130 and 132 for power setting amplifier clocking purposes. The A circuit 118 is also responsive to a power down signal 134 identified as A1P. The B circuit 126 is responsive to a power down circuit 136 designated B1P. The power down signals 134 and 136 are provided by the power down logic of Figure 9 as will be explained in more detail hereinafter. The A coefficient and B coefficient circuits alter the transfer function of the filter 116 to adjust the output of the driver 102 to match the inverse of the transmission line frequency response and reduce ISI. The filter coefficients are alterable in arbitrarily small increments and matched to others to adapt to the power setting circuit to a variety of transmission media.

Page 8, second and third paragraph, REPLACE as follows:

Self-induced ISI in the driver 102 is compensated by a A-coefficient level driver compensation circuit 138 and a ~~driver~~ B coefficient level driver compensation circuit 140 coupled to a driver summing node 141 for the driver 102. The A compensation level circuit is responsive to the mirror current supplying 104 and the A1, A2, and ~~A3~~ **A4** control signals 122. Likewise, the ~~driver~~ B compensation **level** circuit 140 is responsive to the current mirror supply and the B1, B2 and ~~B3~~ **B4** control signals 124. The operation of the compensation circuits 138 and 140 will be described in conjunction with Figures 8 and 8A.

Page 9 second and third paragraph that continues to page 11, REPLACE as follows:

In Figure 3, a bias circuit 300 responsive to a power down signal 301 and a power in signal 303 provides an output as the current mirror supply 104 and a bias supply 305. The bias supply is provided to storage circuits included in the filter 116 (to be described in conjunction with Figure 4). The power down signal at 301 operates transistor P1 and T22 to alter a bias voltage for a current supply 307 connected to the mirror end terminal 104 and the bias terminal 305. A signal at the power in terminal 303 controls a voltage divider 309 to select the appropriate voltage for bias terminal 305 and the input to the current circuit 307. The bias circuit

300 is of the type including feedback to set a voltage that is labeled CBIAS. The CBIAS signal provides a biasing voltage to the gates of P-channel transistors. These ~~forms~~ **form** a mirroring circuit that supplies a controlled current as a reference to the output current source mirrors in the driver.

In Figure 4, the FIR filter 116 includes the A coefficient setting circuit 118 and the B coefficient circuit 126, both connected to the transmission line 114. Each coefficient setting circuit has a series of cascaded Z delay stages to be explained in more detail in connection with Figures 5 and 6. The A coefficient setting circuit 118 includes stages 501, 503, 505 and 507, each stage providing unit delay Z^N. The B coefficient setting circuit 126 includes stages 601, 603, 605, and 607, each stage providing unit delay Z^N. Obviously, the A and B circuits can comprise more or less stages depending on the characteristics of the transmission line 114. Each A coefficient setting stage 501...507 is linked to a three stage shift register 701, 703, and 705, 707 which provide control signals Q2 and Q2N to the coefficient setting circuits 501,....507. Likewise, The B coefficient setting stages 601...607 are linked to 3 ~~satage~~ **stage** shift register 702, 704, 706 and 708 which provide control signals Q2,4, Q4N to B coefficient setting circuits 601...607. True complement controls signals Q1 and Q1N are generated in one stage of each shift register and provided to the power setting circuit shown in Figure 2. The shift registers will be described in conjunction with Figures 7A, 7B, and 7C. A data signal 401is fed to each shift register in cascade which create the delay increments $Z^{-1},\ldots, Z^{-n}$ for the A and B coefficient setting circuits. A data output 711 is taken from the A coefficient setting circuits at terminal 403. Amplifiers 405 and 407 are included in the data circuit to create the initial delay unit Z^{-1}. The present output of each storage circuit equals its preceding input. The filter transfer function is of the general form of $H(Z) = AB_0+AB_1Z^{-1}+BA_2Z^{-2}+AB_nZ^{-n}$. The numerical values of the A and B coefficients are set by input values to the A and B coefficient setting circuits. A determining factor for the values of the A and B coefficients include the characteristics of the transmission media, the speed of transmission, the type of back plane and the type of chip packages connected to the backplane. The general details of the Z transform for filter116 are described in the text both "Introductory Digital Signal Processing with Computer Applications" by Paul A. Lind et al., published by John Wiley & Sons, New York, NY, May 1990 (ISBN 0471915645) PBK, Chapters 4 and 5, which are fully incorporated herein by reference.

Page 11, second paragraph REPLACE as follows:

In Figure 5, the ~~driver~~ A coefficient setting circuit 118 is coupled to the transmission lines 114 and includes coefficient stages 501, 503, and 505, responsive to control signal A1 at terminal 502; control signal A2 at terminal 504, and control signal A4 at terminal 506. The programmable input control signals A1, A2, A4 in conjunction with Q2 and Q2N control signals at terminals 509 and 511 alter the output of both sides of the differential signal appearing on the transmission lines 114. The effect of the control signal or coefficients is to modify the frequency response of the driver according to the H (Z) transfer function.

Page 15, first and second paragraphs, REPLACE as follows:

In Figure 8, the coefficient level ~~driver~~ compensation circuit 138 assists in the elimination of driver-induced intersymbol interference. The circuit 138 includes three stages, each stage responsive to a programmable control pulse A1 at terminal 801; A2 at terminal 803; and A4 at terminal 805. The control signals ~~A1,~~ A2 and A4 are the same as provided to the A coefficient setting circuit 118. Mirror current supply 104 is also provided as an input to each stage. The control signals in combination with the Q1, Q1N (true/complement) control signals provided to the driver, function to alter the current on the transmission line 114 provided by the current amplifier 217 shown in Figure 2. By lowering the driver current, the induced intersymbol interference is reduced and the bandwidth increased.